EE 505

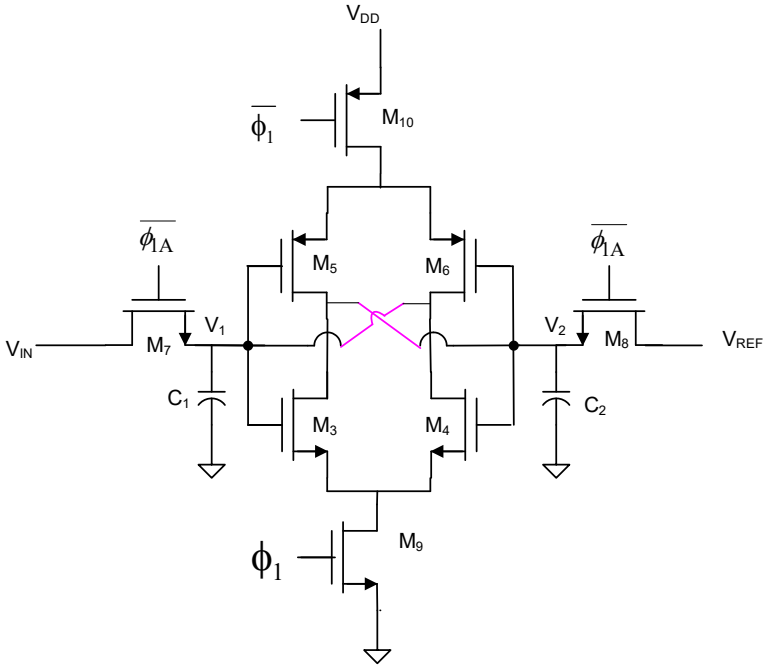
Lecture 20

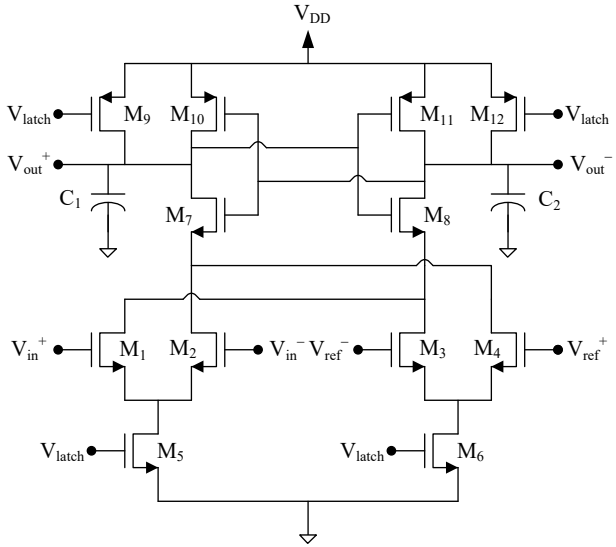
ADC Design

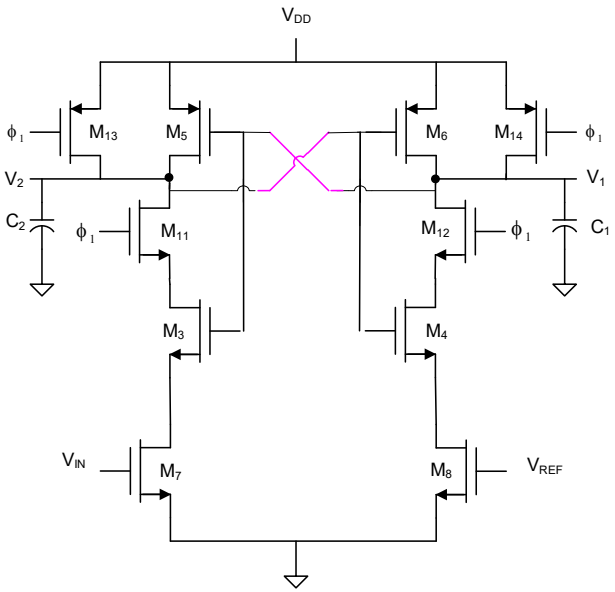
- The Flash ADC
- Comparators
- Interpolating ADCs
- Folded ADCs

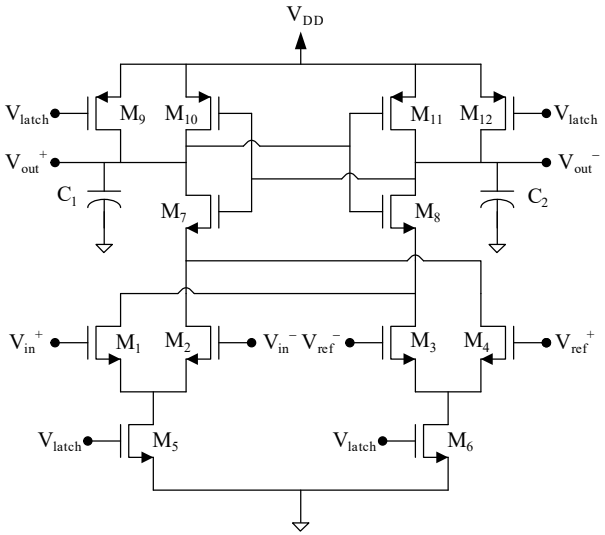
Review from Last Lecture

Clocked Comparator with Regenerative Feedback









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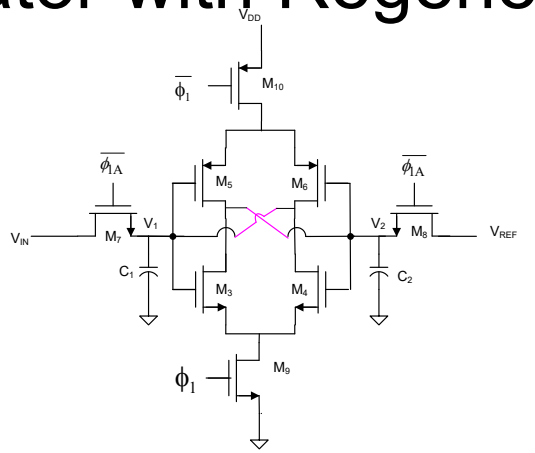
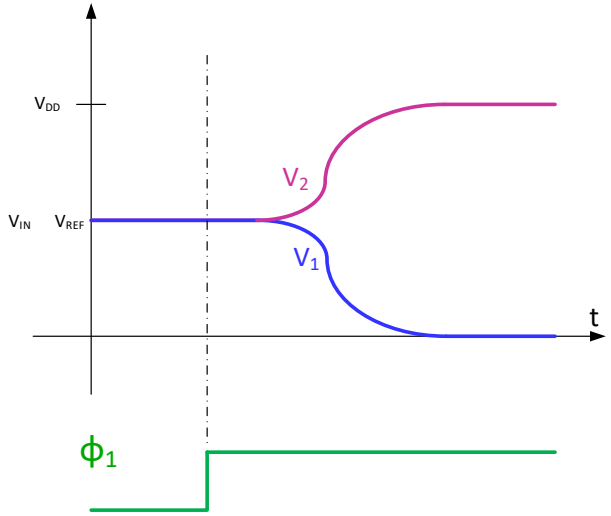
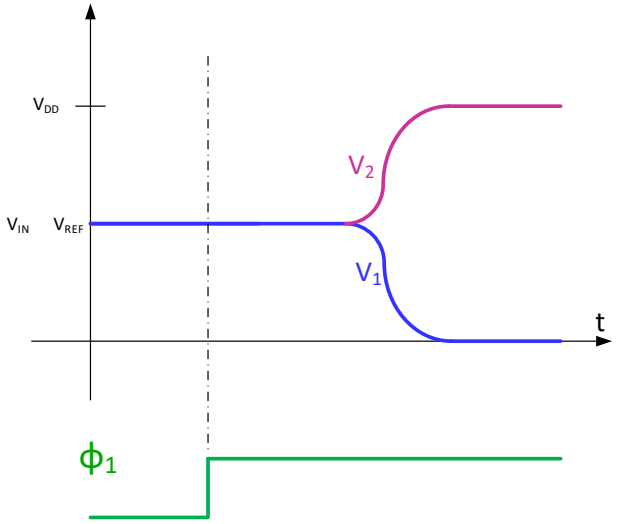


when V_{IN} and V_{REF} close to each other

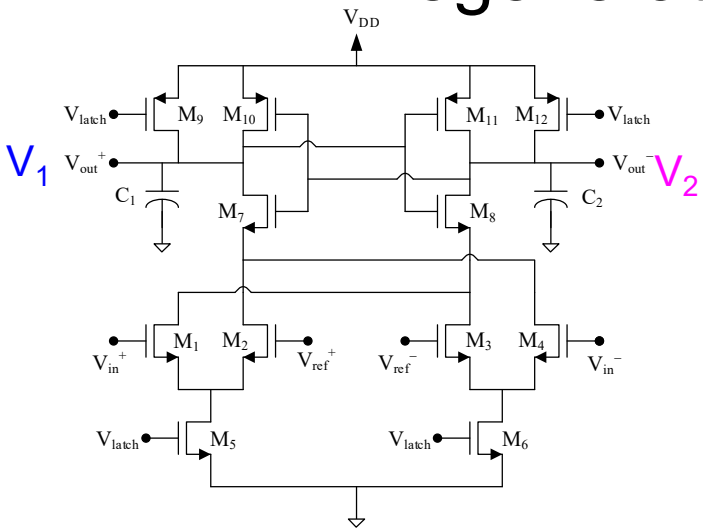


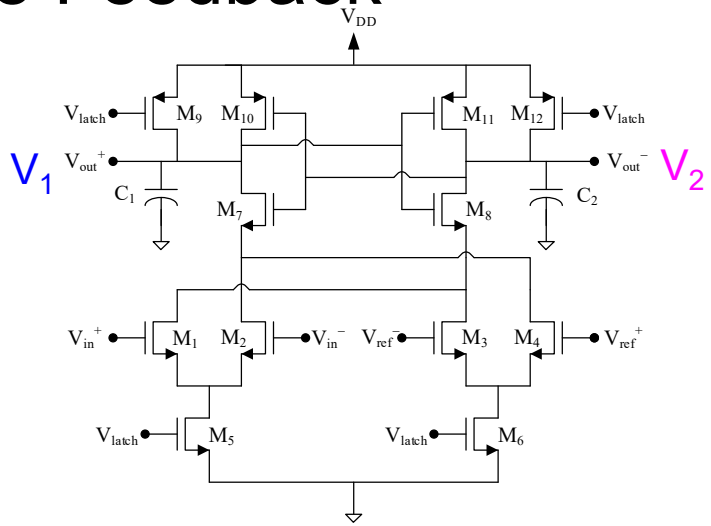


- decision delayed
- may stay in metastable state until after decision must be made
- vulnerable to making wrong decision due to offset or noise

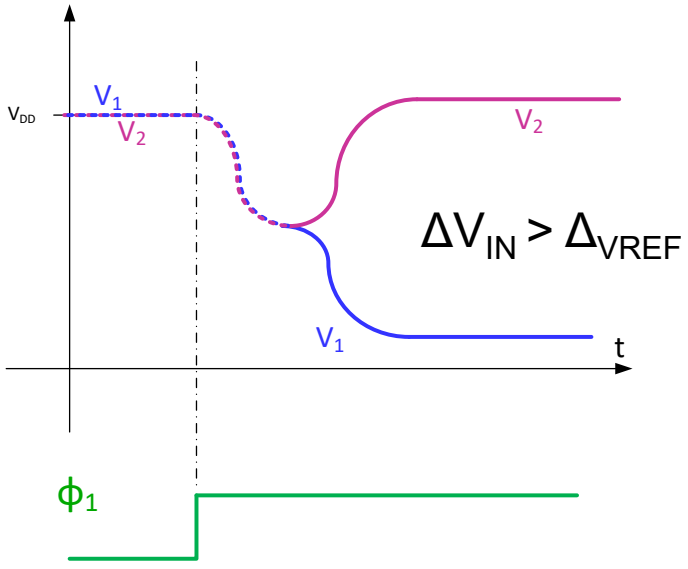
Review from Last Lecture

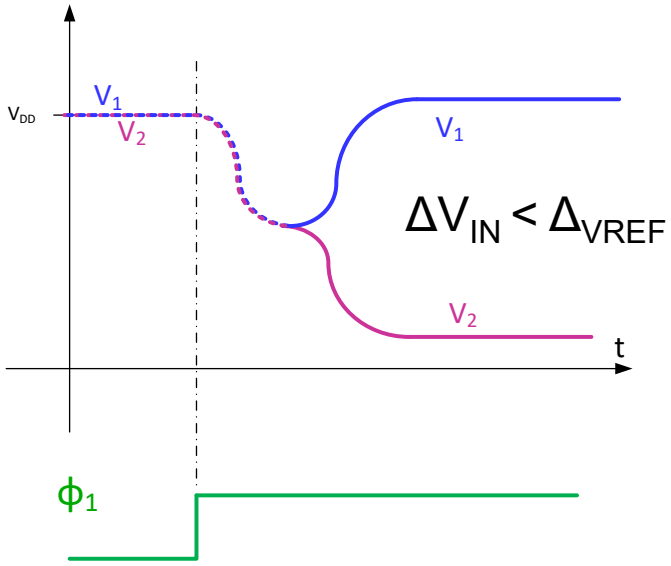
Katyal and Halonen Comparators with Regenerative Feedback



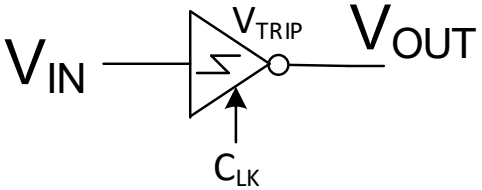


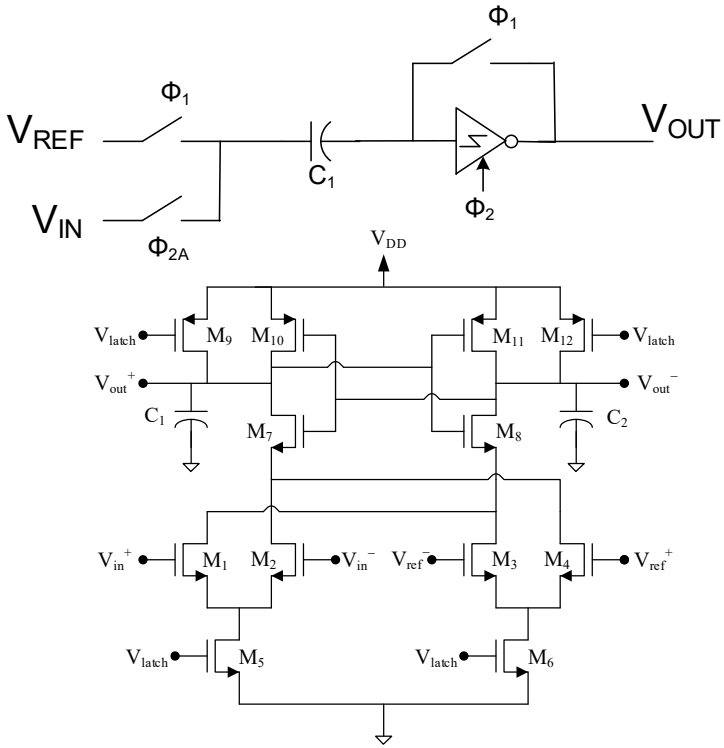
Ideal Responses

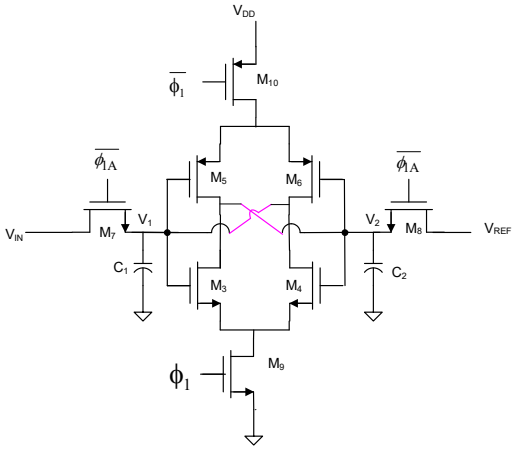




Where are poles of regenerative comparators located?







In RHP !

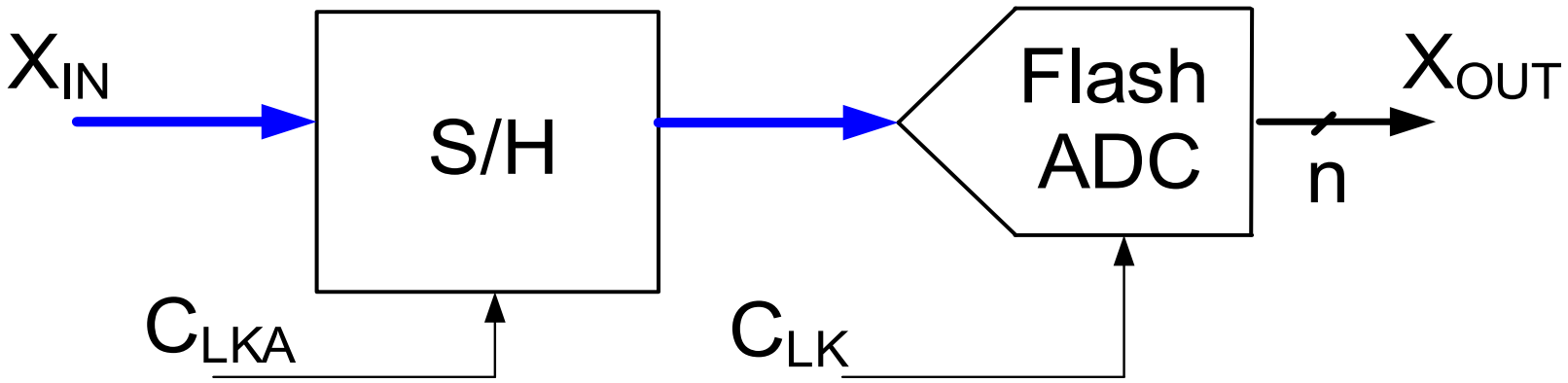
Is stability of concern?

No ! Want positive real axis poles (i.e. unstable circuit) to force decision

Review from Last Lecture

Input change during conversion

Front-End S/H can mitigate effects of input change during conversion

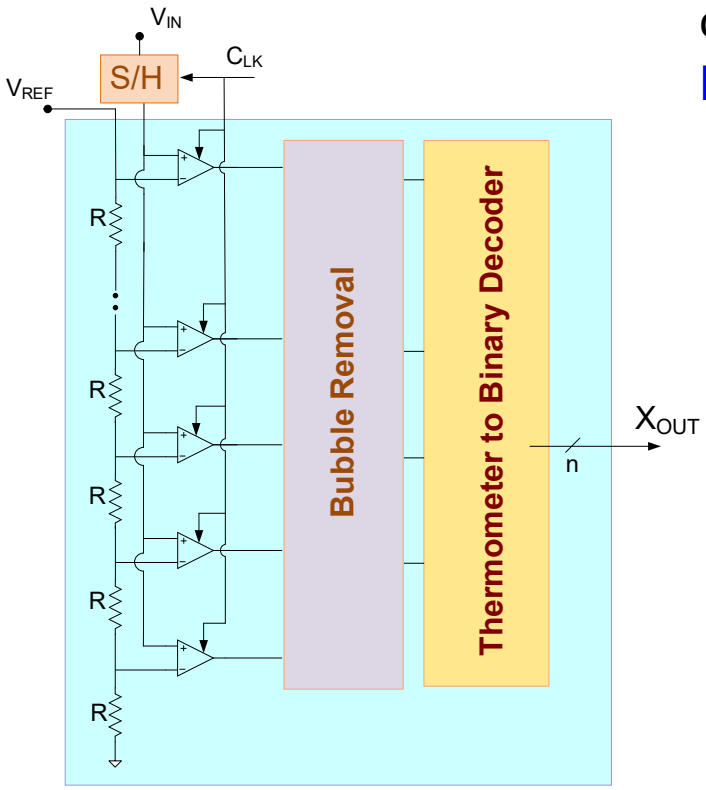


- Speed of sample/hold of concern
- Noise of S/H
- Nonlinearity of S/H
- Input range of S/H
- Power dissipation of S/H
- Loose asynchronous operation of ADC
- Widely used

⇒ S/H may be most challenging part of design

Will discuss input S/H later

Flash ADC



Basic structure has thermometer code at output

Performance Issues:

- \+ Very fast
- \+ Simple architecture
- \+ Instantaneous output
- Bubble vulnerability
- Input change during conversion
- Offset of comparators
- Number of components and area (for large n)
- − Speed of comparators
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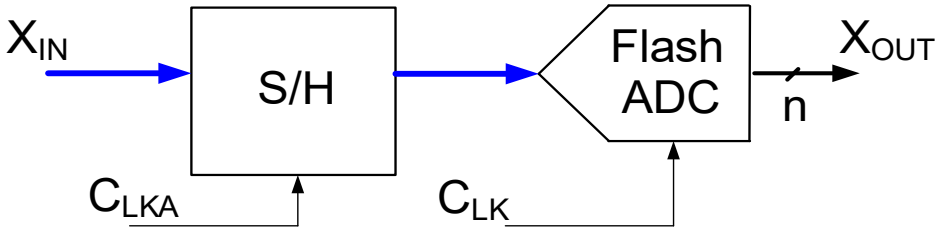
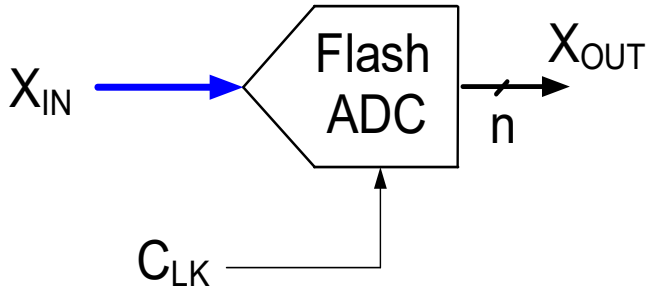
Input change during conversion



Can we clock only the comparators in a Flash ADC thereby eliminating the S/H?

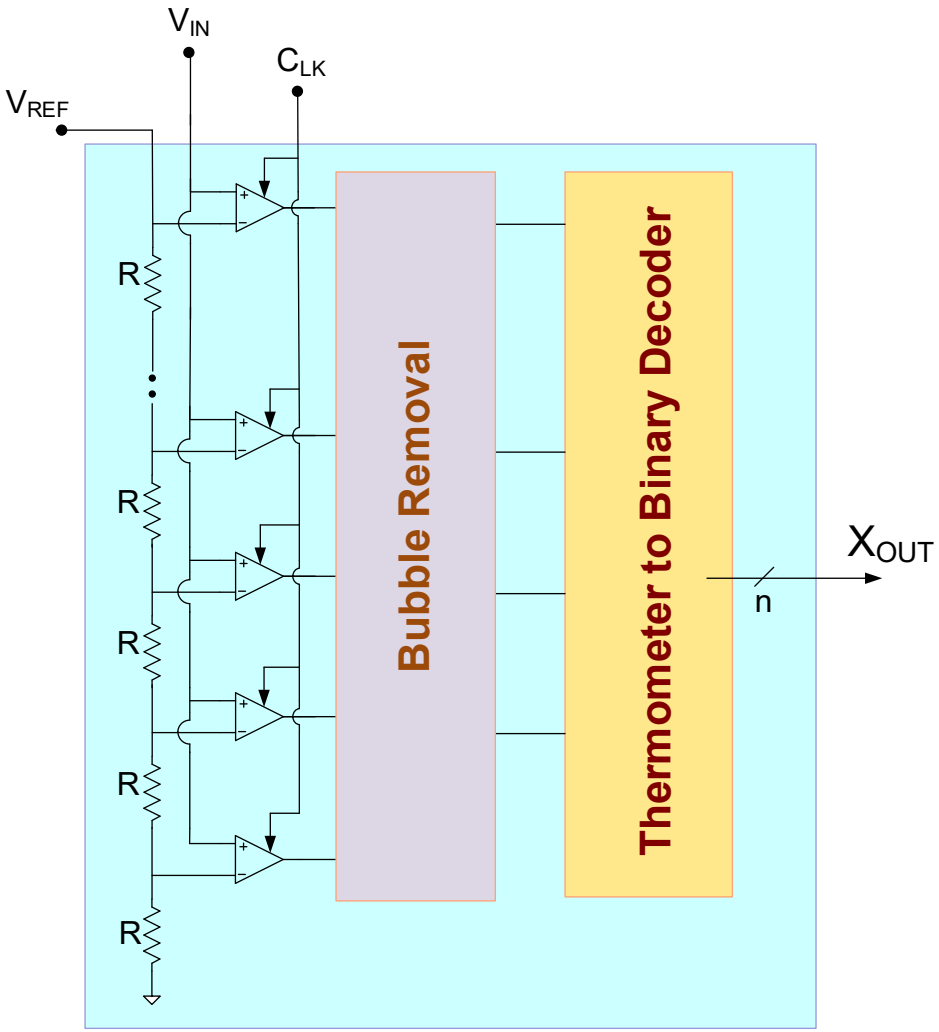


Clocking of Comparaors Only

- Extremely tight requirements on CLK generator and Input propagation
- Clocking of pre-amps may not be easy to do
- Some switched-capacitor comparators may have inherent S/H of the input

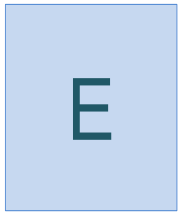
Input change during conversion

Clock of Comparators only instead of input S/H in Flash ADC

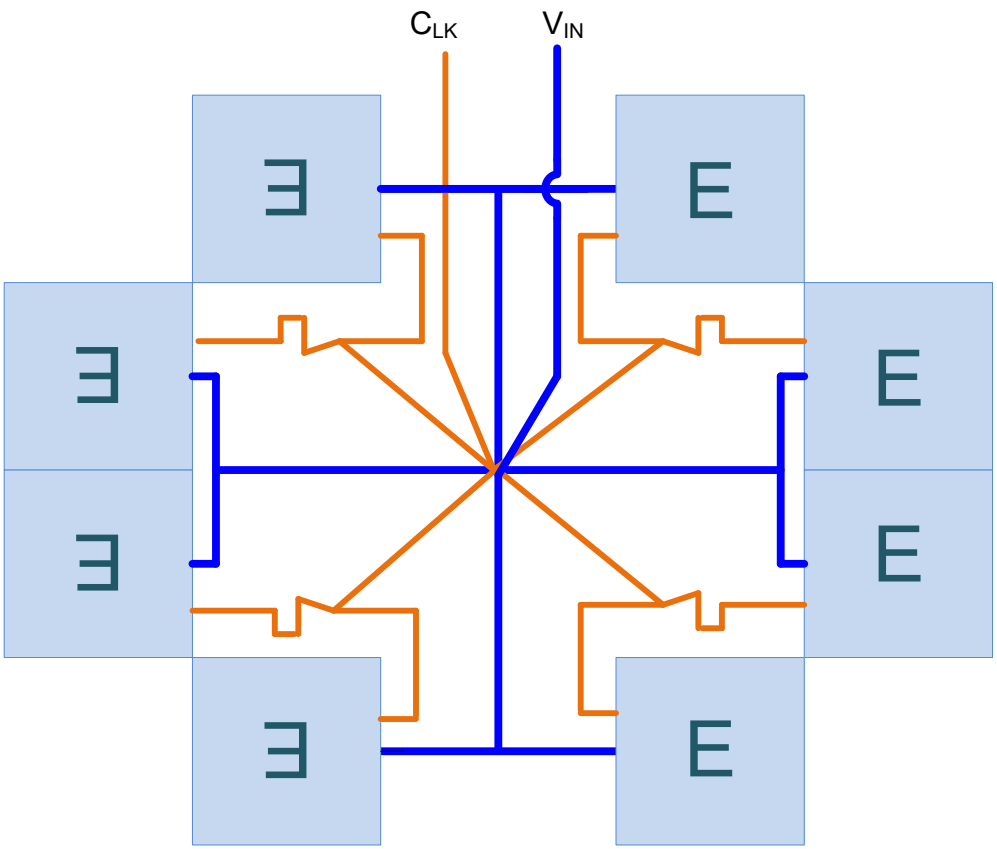


Input change during conversion

Routing of Clock and Input is Critical



Comparator



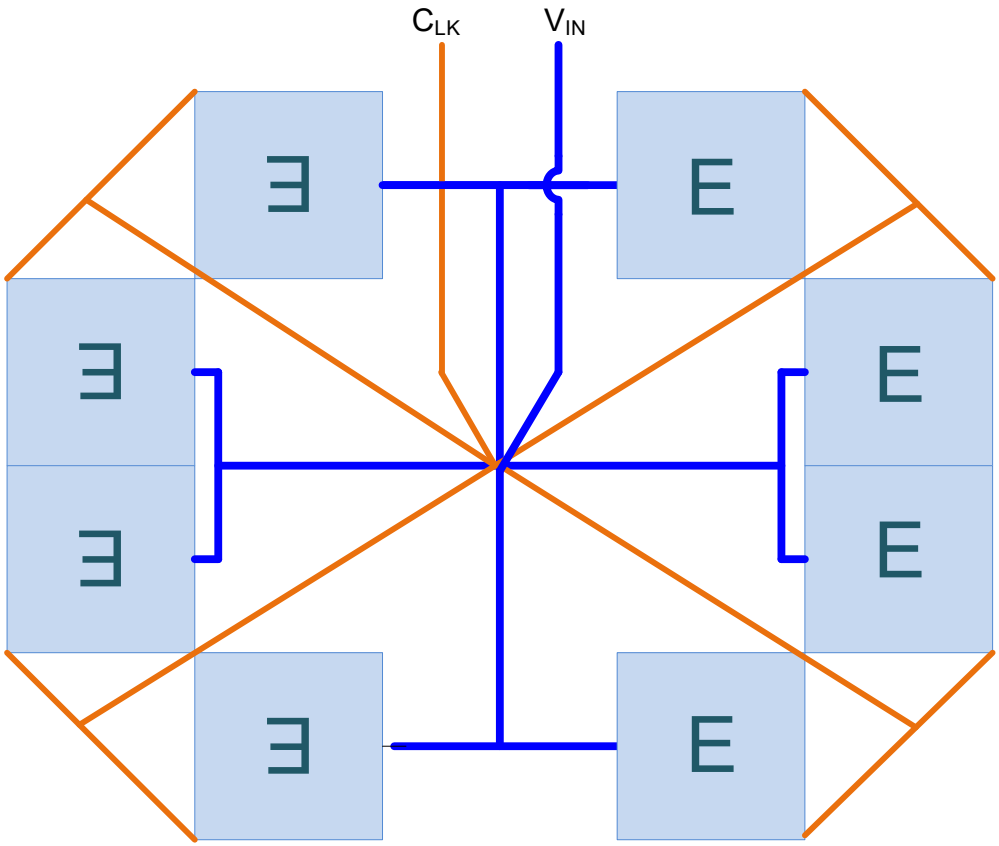
Symmetric Equal Path Length Layout

Path length of V_{IN} and C_{LK} need not be identical but convenient if they are

Have maintained minimal overlap of V_{IN} and C_{LK}

Input change during conversion

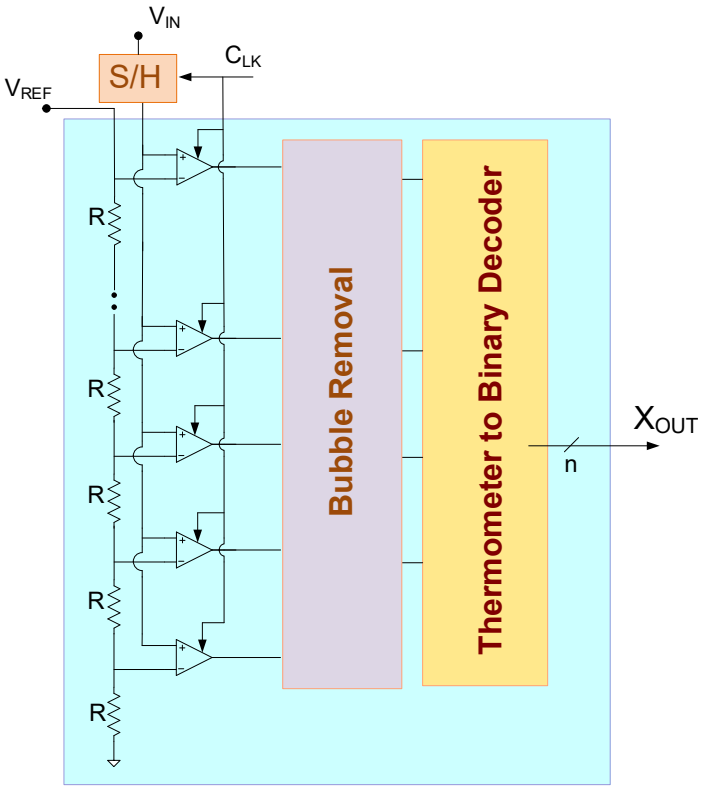
Routing of Clock and Input is Critical



Symmetric Paths for V_{IN} and C_{LK}

Layout challenging if resolution is very large

Flash ADC



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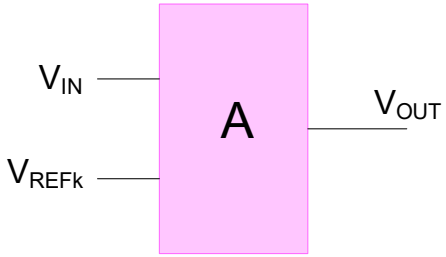
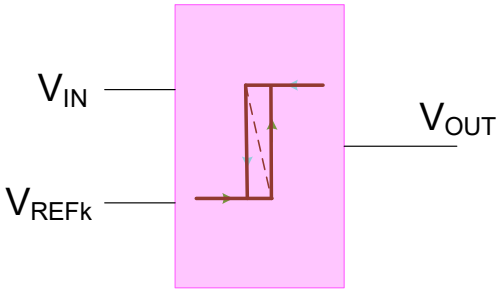
Speed of Comparators

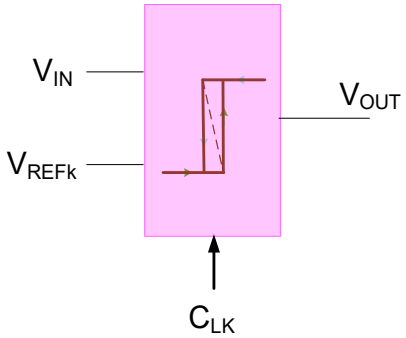


Linear Amplifier as Comparator

- Gain may be inadequate to generate Boolean output for some inputs (metastability)
- Common-mode input varies significantly with V_{REFk}

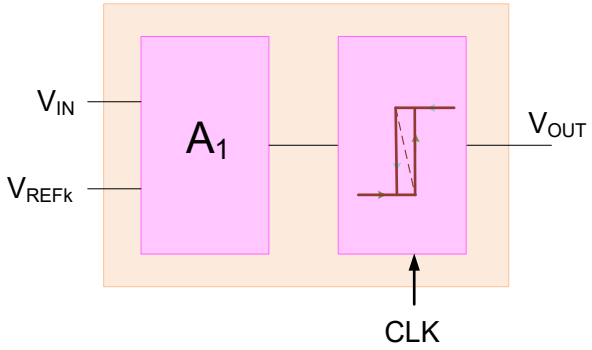
Regenerative Feedback Comparators





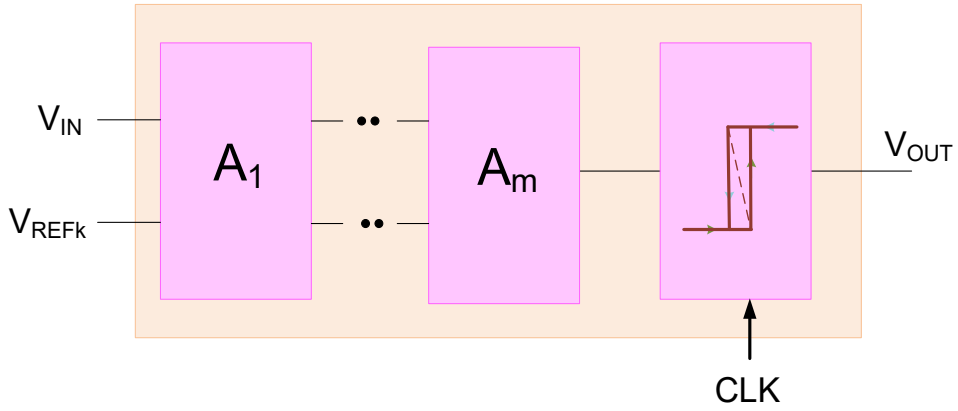
- Reduces (but does not eliminate) metastability concerns
- Common-mode input still varies with V_{REFk}
- Offset Voltage High
- C_{LK} can significantly improve speed
- C_{LK} can force operation on negative slope region thereby reducing hysteresis window-induced previous code dependence
- Kickback to Input of concern

Speed of Comparators



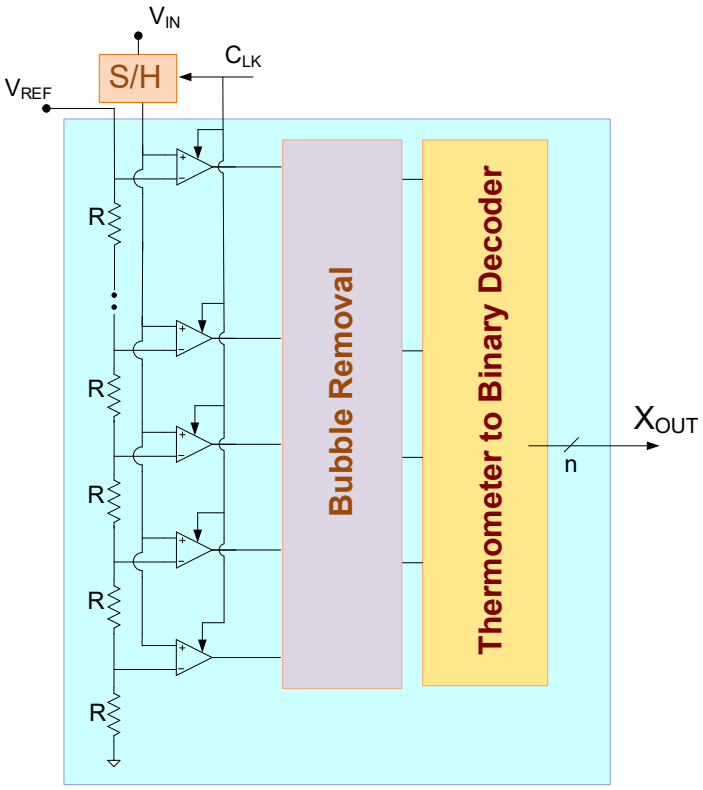
- Preamp often precedes regenerative stage
- Regenerative stage can be single-ended or differential
- Common-mode input to preamp still of concern
- Common-mode inputs of all regenerative stages can be the same
- Significant reduction in offset voltage possible
- Kickback to V_{IN} and V_{REFk} can be reduced

Speed of Comparators



- Two or more stages of preamp gain often used
- Further reduces offset voltage and metastability concerns
- Number of stages can be selected to optimize speed and power
- Common-mode input in all stages after first can be the same

Flash ADC



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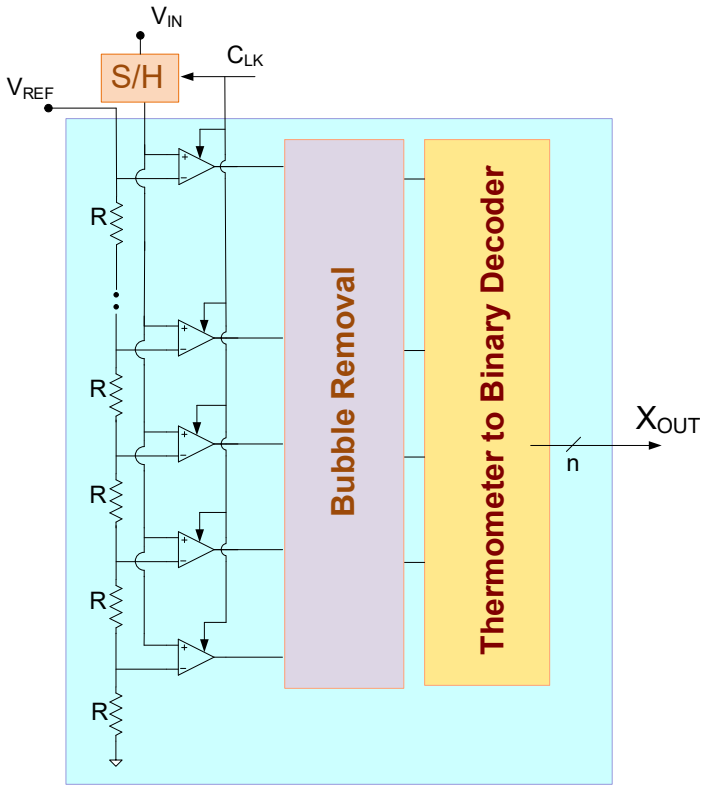
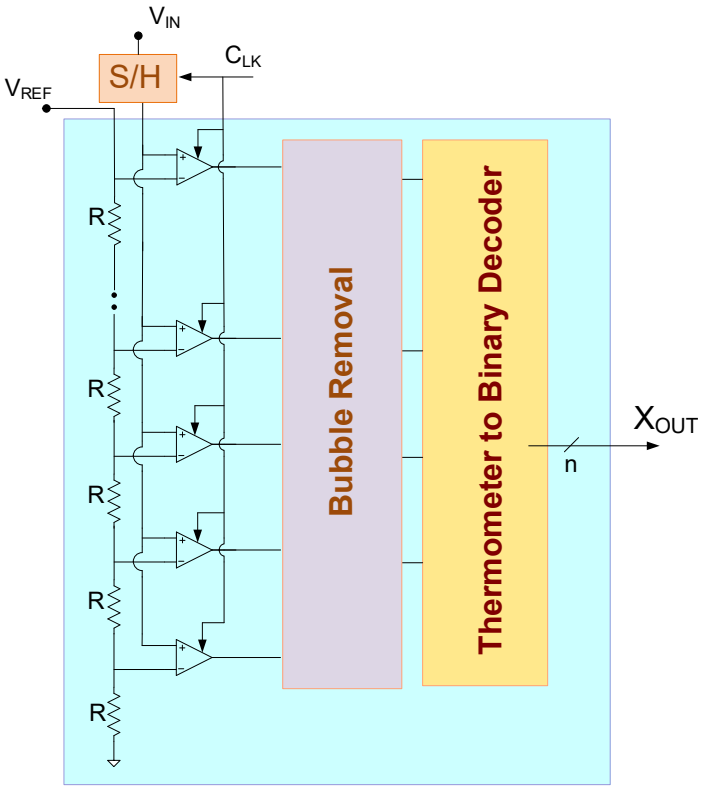
Loading of V_{REF} and V_{IN}



- Capacitive load on V_{IN} is large for large n
- Resistors in R-string small for fast recovery when V_{IN} changes
- Inductance on bonding leads for V_{REF} of concern if V_{REF} externally generated
- Output impedance must remain low at high frequencies if V_{REF} internally generated

Flash ADC



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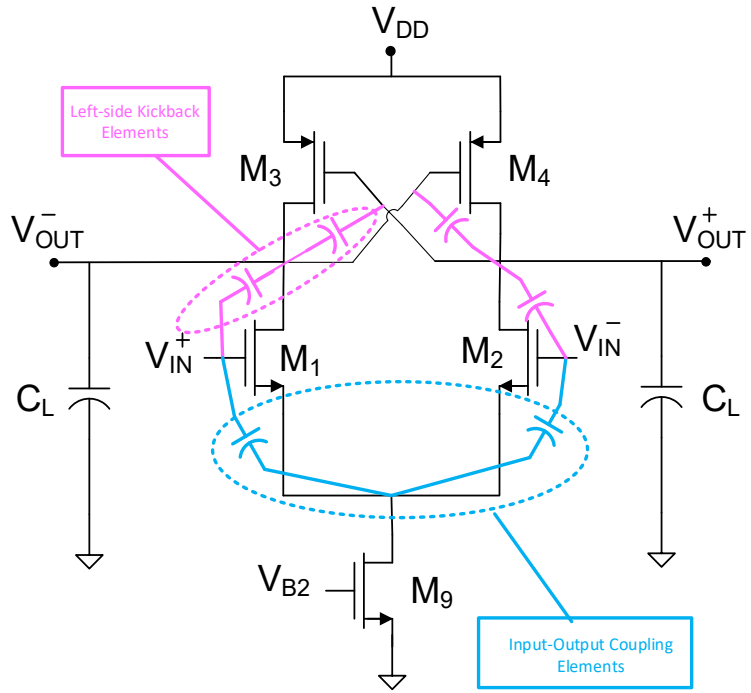
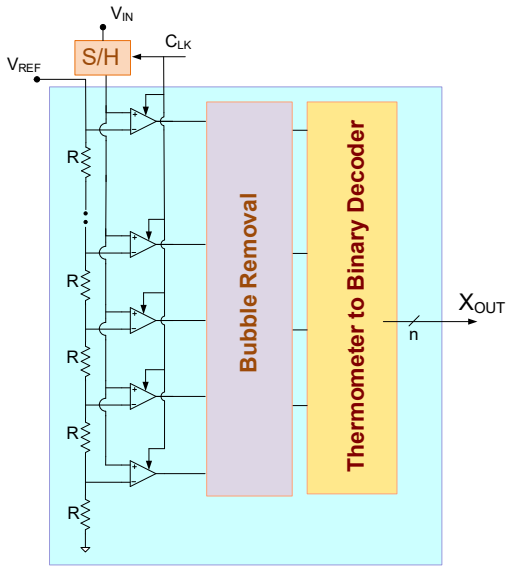
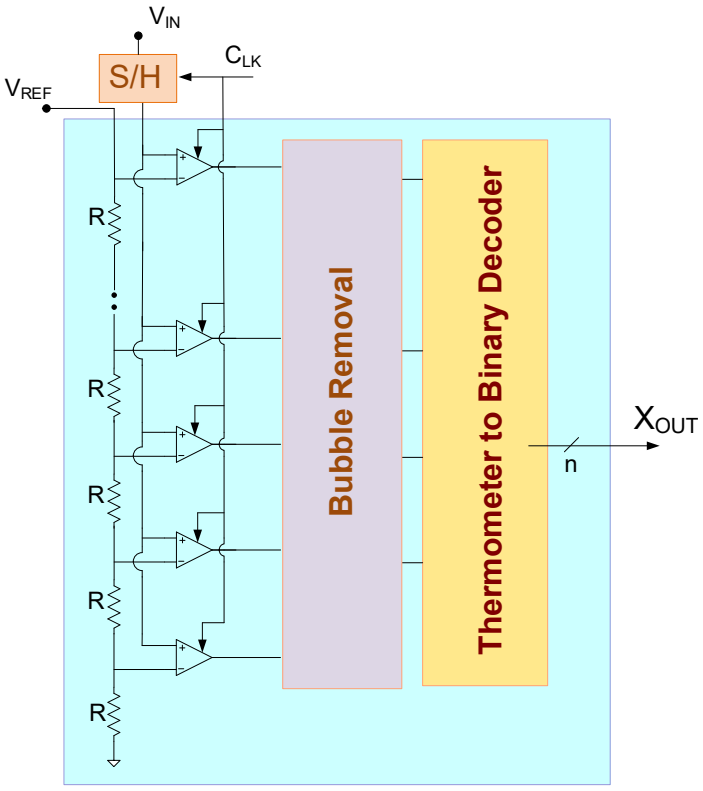
Propagation of V_{IN} and Kickback





- Key decisions being made by comparators near 0-1 thermometer code transition
- Several comparators often changing states during each conversion introducing lots of kickback
- Kickback can be reduced by introducing preamp
- Input-output coupling on each comparator introduces large transients in R-string for large input changes
- Delay in V_{IN} propagating down string but introducing delay in clock can mitigate concern

Flash ADC



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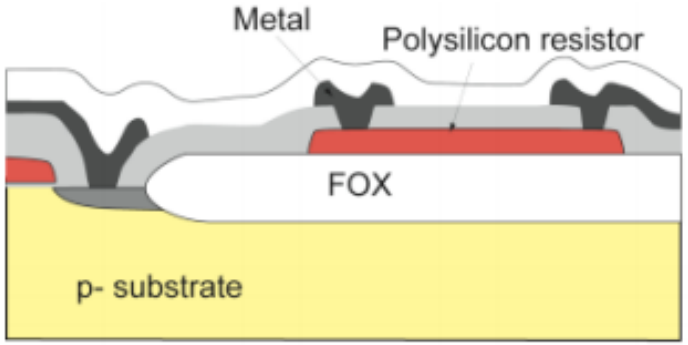
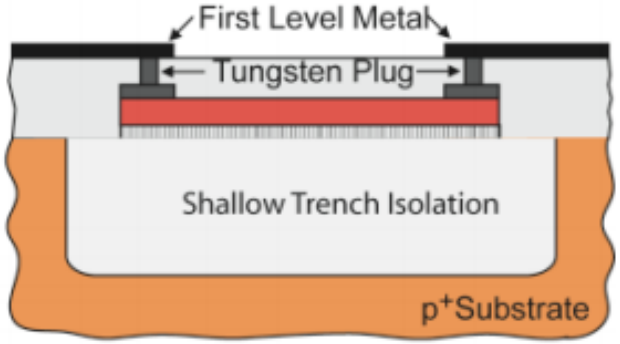
Voltage and temperature dependence of R's

From lecture notes of Phil Allen

Polysilicon Resistor



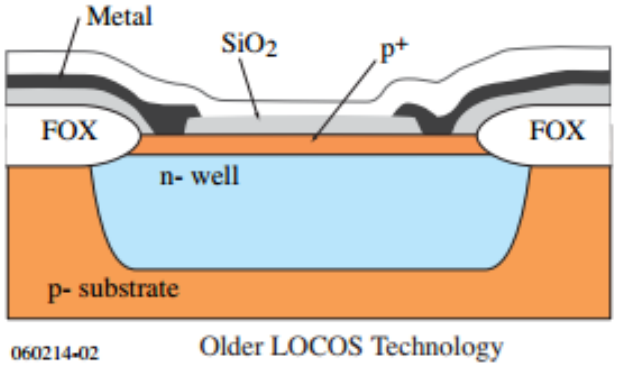


30-100 ohms/square (unshielded)
100-500 ohms/square (shielded)
Absolute accuracy = ±3 0%
Relative accuracy = 2% (5 μm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V

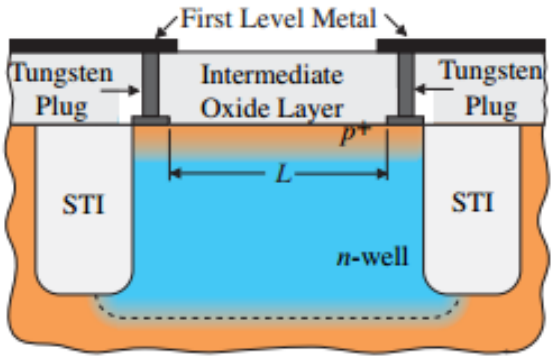
Voltage and temperature dependence of R's

From lecture notes of Phil Allen

MOS Resistors - Source/Drain Resistor



Older LOCOS Technology



Diffusion:

10-100 ohms/square
Absolute accuracy = ±35%
Relative accuracy=2% (5μm), 0.2% (50μm)
Temperature coefficient = +1500 ppm/°C
Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

500-2000 ohms/square
Absolute accuracy = ±15%
Relative accuracy=2% (5μm), 0.15% (50μm)
Temperature coefficient = +400 ppm/°C
Voltage coefficient ≈ 800 ppm/V

Comments:

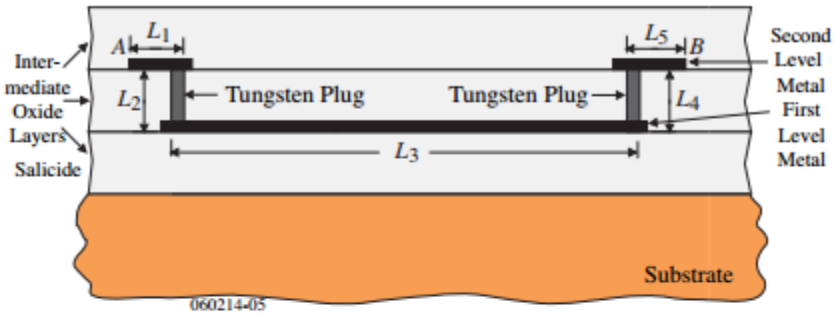
- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

Voltage and temperature dependence of R's

From lecture notes of Phil Allen

Metal as a Resistor

Illustration:



Resistance from A to B = Resistance of segments L_1, L_2, L_3, L_4, and L_5 with some correction subtracted because of corners.

Sheet resistance:

50-70 mΩ/□ ± 30% for lower or middle levels of metal

30-40 mΩ/□ ± 15% for top level metal

Watch out for the current limit for metal resistors.

Contact resistance varies from 5Ω to 10Ω.

Tempco ≈ +4000 ppm/°C

Need to derate the current at higher temperatures:

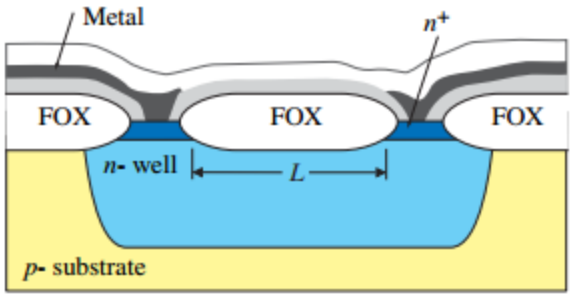
$$I_{DC}(T_j) = D_t \cdot I_{DC}(T_r)$$

T_j(°C)	T_r(°C)	D_t
<85	85	1
100	85	0.63
110	85	0.48
125	85	0.32
150	85	0.18

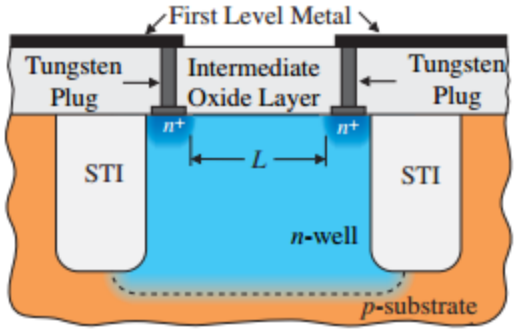
Voltage and temperature dependence of R's

From lecture notes of Phil Allen

N-well Resistor



060214-04 LOCOS Technology



1000-5000 ohms/square
Absolute accuracy = ±40%
Relative accuracy ≈ 5%
Temperature coefficient = 4000 ppm/°C
Voltage coefficient is large ≈ 8000 ppm/V
Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent
- Could put a p^+ diffusion into the well to form a pinched resistor

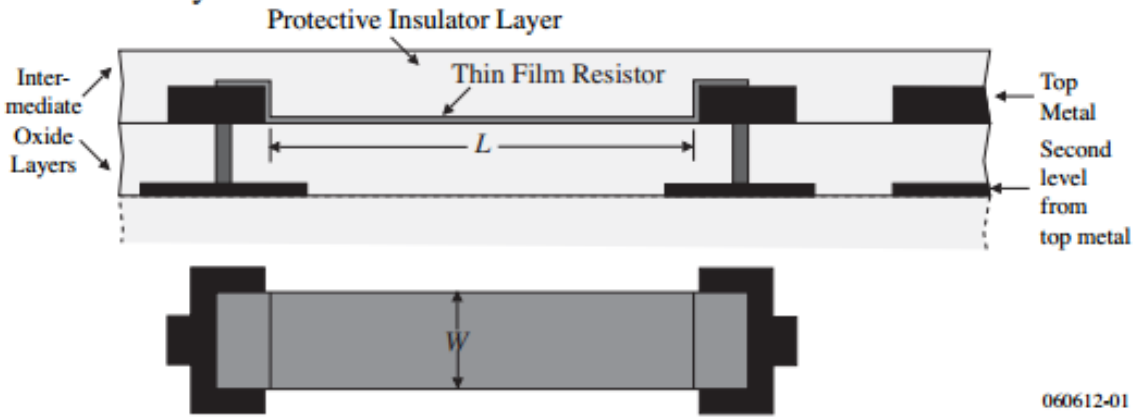
Voltage and temperature dependence of R's

From lecture notes of Phil Allen

Thin Film Resistors

A high-quality resistor fabricated from a thin nickel-chromium alloy or a silicon-chromium mixture.

Uppermost metal layer:



Performance:

Sheet resistivity is approximately 5-10 ohms/square

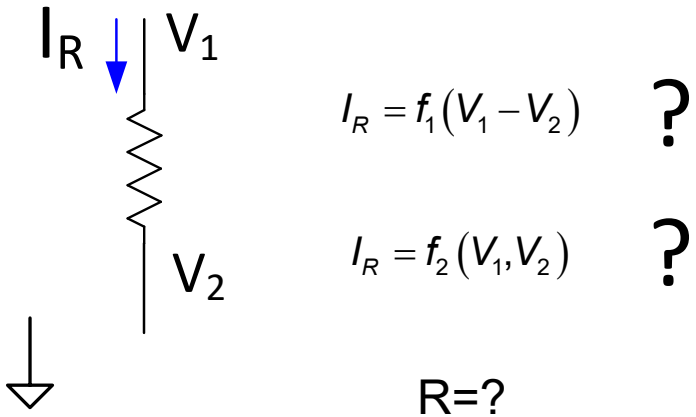
Temperature coefficients of less than 100 ppm/°C

Absolute tolerance of better than ±0.1% using laser trimming

Selectivity of the metal etch must be sufficient to ensure the integrity of the thin-film resistor beneath the areas where metal is etched away.

Voltage and temperature dependence of R's

Be careful with characterization of voltage coefficients of resistors – simulators probably can not be completely trusted !



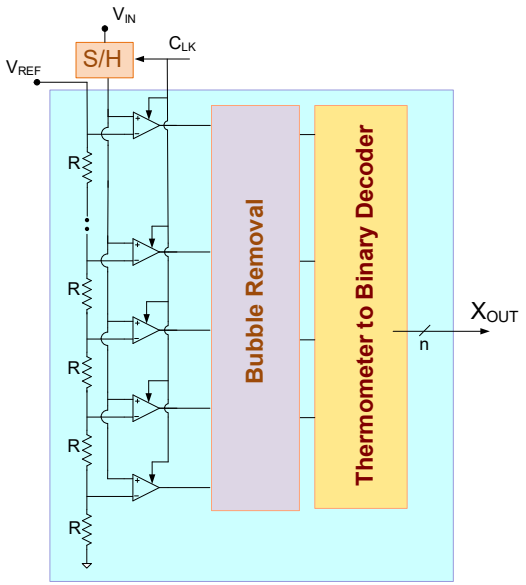
Modeling Diffusion Resistors

Ken Kundert
Designer's Guide Consulting, Inc.

The issues:

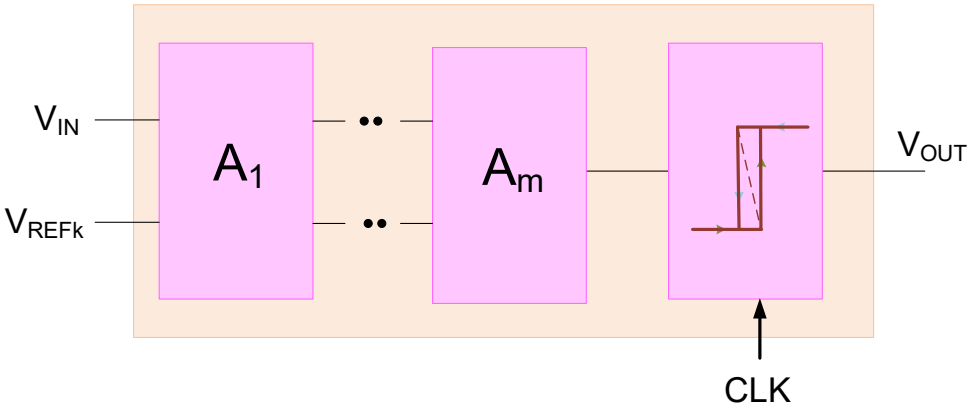
- How is resistance actually defined when I-V relationship is not linear
- Are integrated resistors 2-terminal or 3-terminal devices?

Interpolating ADC

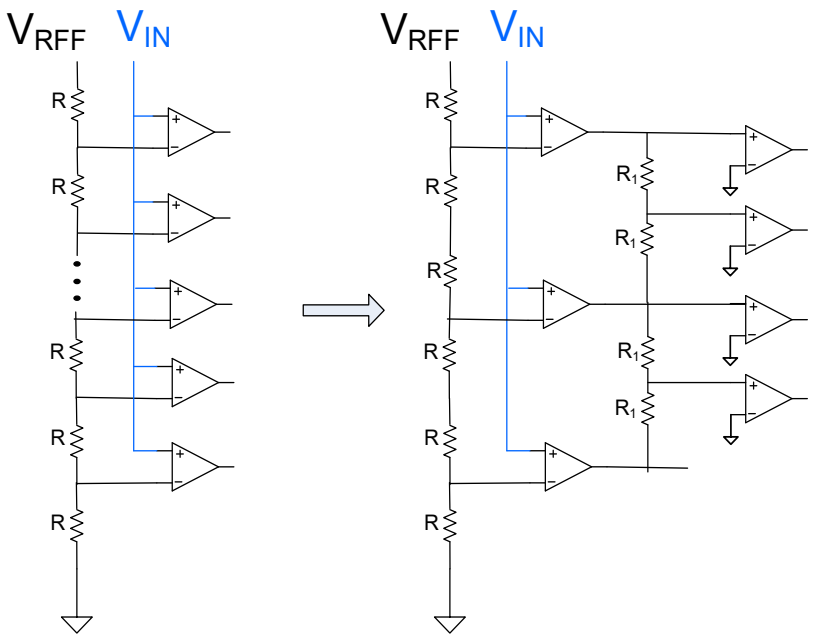


Full Flash ADC

- Key decisions being made by comparators near 0-1 thermometer code transition in Flash ADCs
- Other comparators (away from key decision region) consume power and area but provide little useful information
- Each regenerative comparator typically requires a preamp stage(s) in full flash ADC



Interpolating Flash ADC



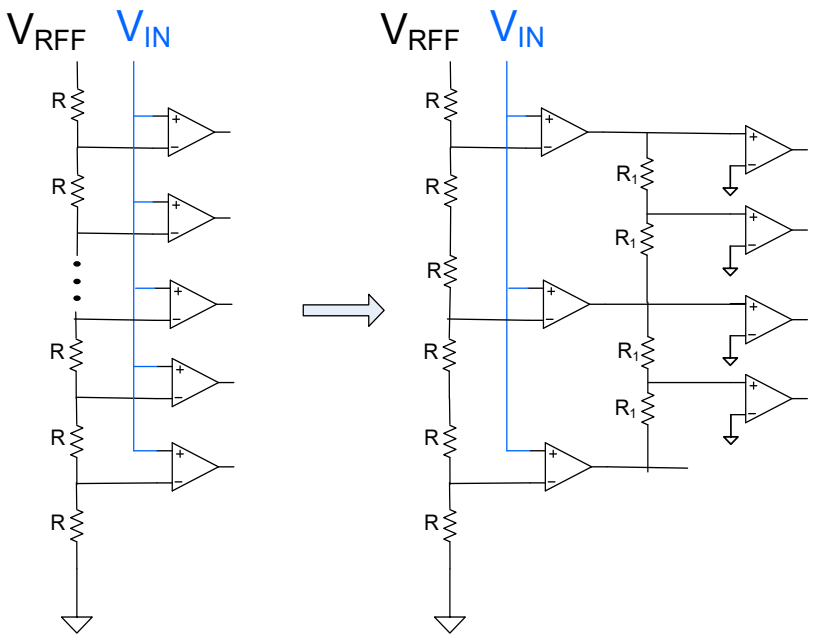
Standard Flash

Interpolated Flash

It may appear that the number of amplifiers/comparators and resistors have been increased but …

- First stage amplifiers/comparators can be a pre-amp
- Second stage comparators can be a latch
- Number of critical resistors in first stage has been decreased (thereby also facilitating common-centroid layout)

Interpolating Flash ADC



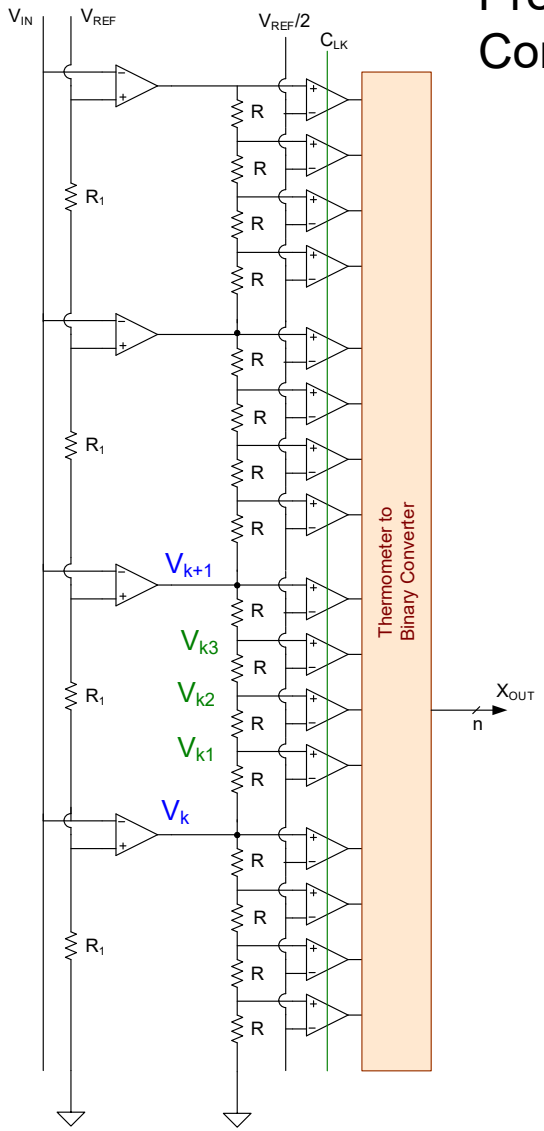
Standard Flash

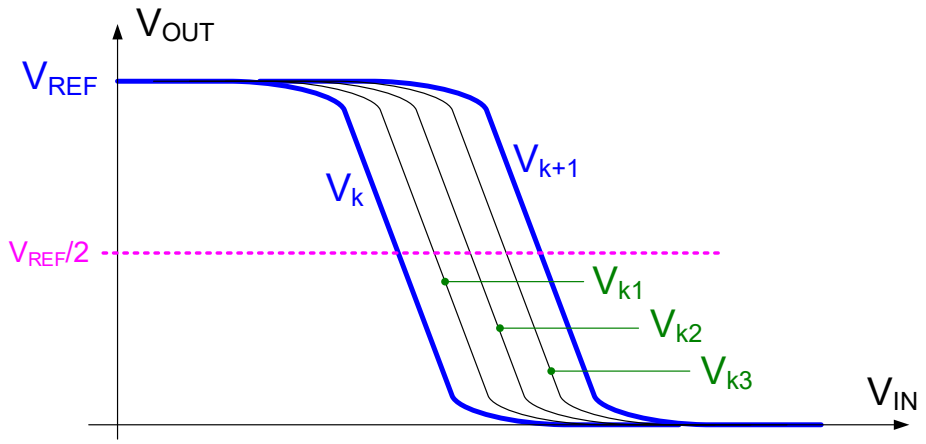
Interpolated Flash

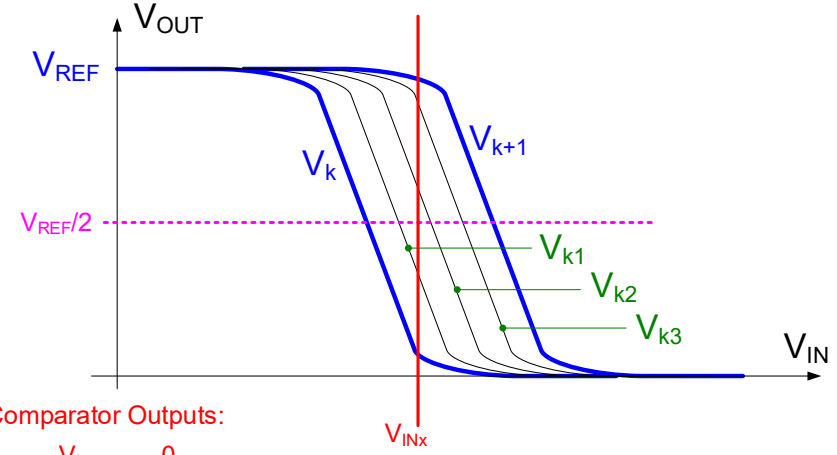
- Reduction in pre-amp area and power
- Latches all referenced to ground
- Loading on V_{IN} reduced
- Kickback to V_{REF} reduced
- V_{IN} coupling to V_{REF} reduced
- Multiple levels can be included in interpolator array

Interpolating Flash ADC

4 –levels of interpolation
Preamp gain not critical
Common mode set at $V_{REF}/2$







Comparator Outputs:

V_k	0
V_{k1}	0
V_{k2}	1
V_{k3}	1
V_{k+1}	1

V_{INk} line really is vertical !

Variants of Interpolating Flash

Patent Number: **5,867,116**

Date of Patent: **Feb. 2, 1999**

Analog Devices

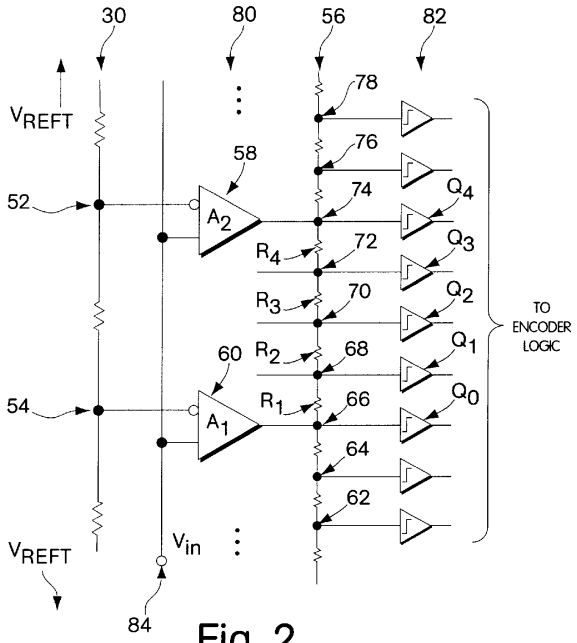


Fig. 2
(PRIOR ART)

Standard R-String Interpolators

Variants of Interpolating Flash

Patent Number: **5,867,116**

Date of Patent: **Feb. 2, 1999**

Analog Devices

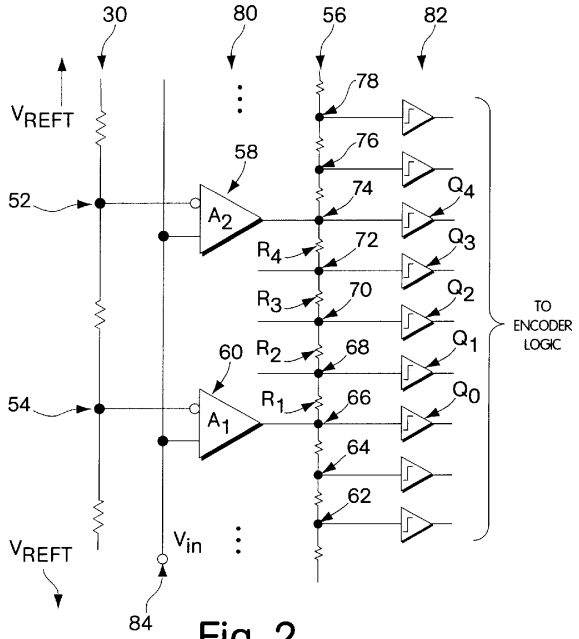
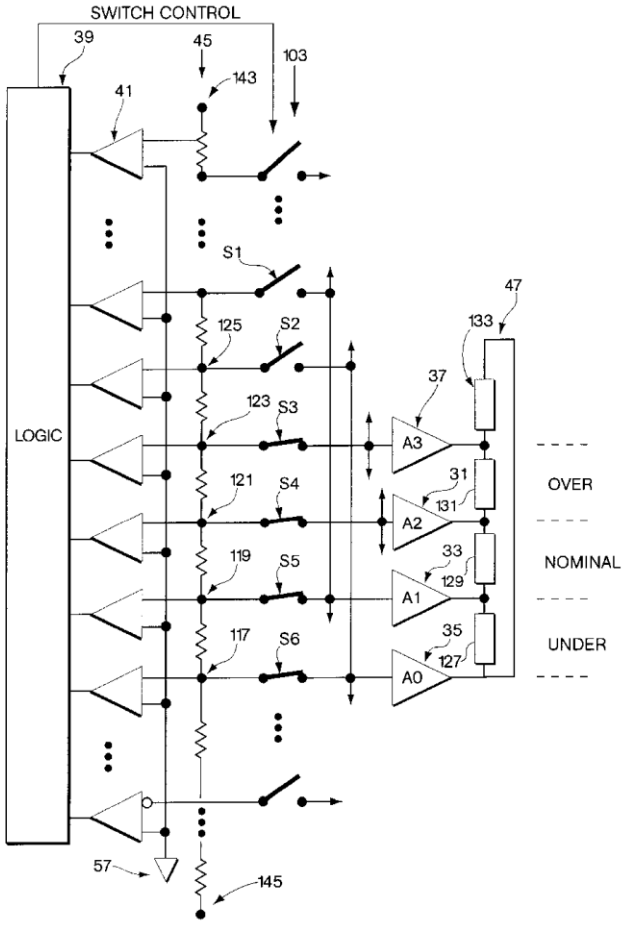


Fig. 2
(PRIOR ART)



Flying Interpolator

Variants of Interpolating Flash

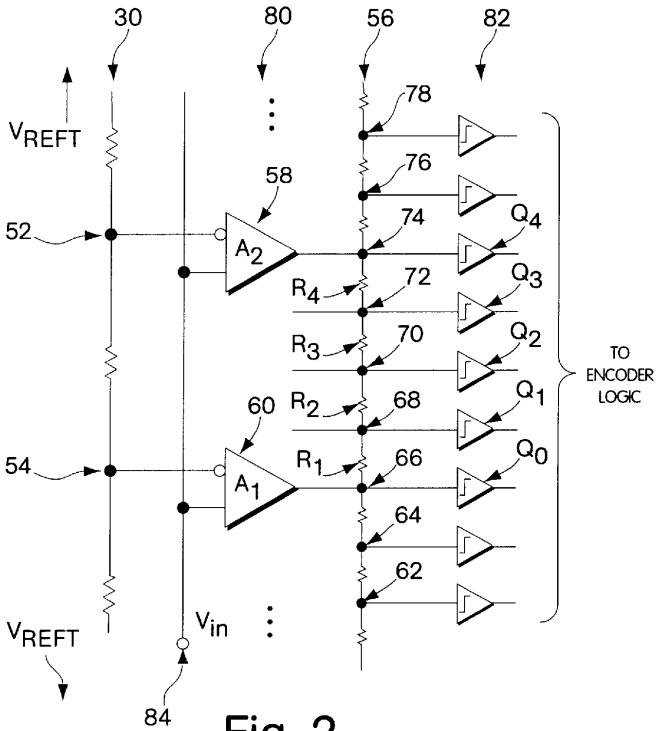


Fig. 2
(PRIOR ART)

Interpolator can be based upon alternative DAC structures

- Current Steering
- Charge Redistribtion

Variants of Interpolating Flash

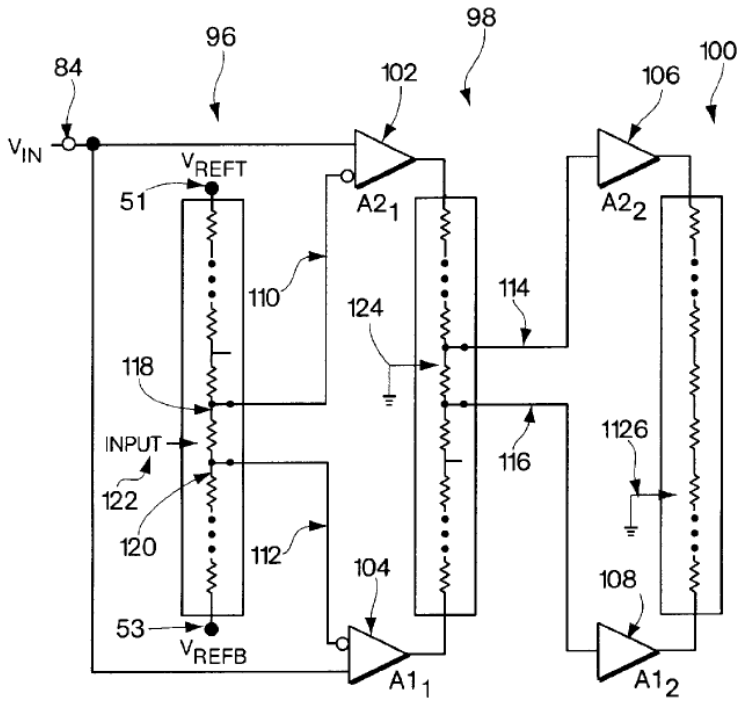


Fig. 11
(PRIOR ART)

Multi-Level Interpolators

Flash ADC Summary

Flash ADC

Very fast

Simple structure

Usually Clocked

Bubble Removal Important

Seldom over 6 or 7 bits of resolution

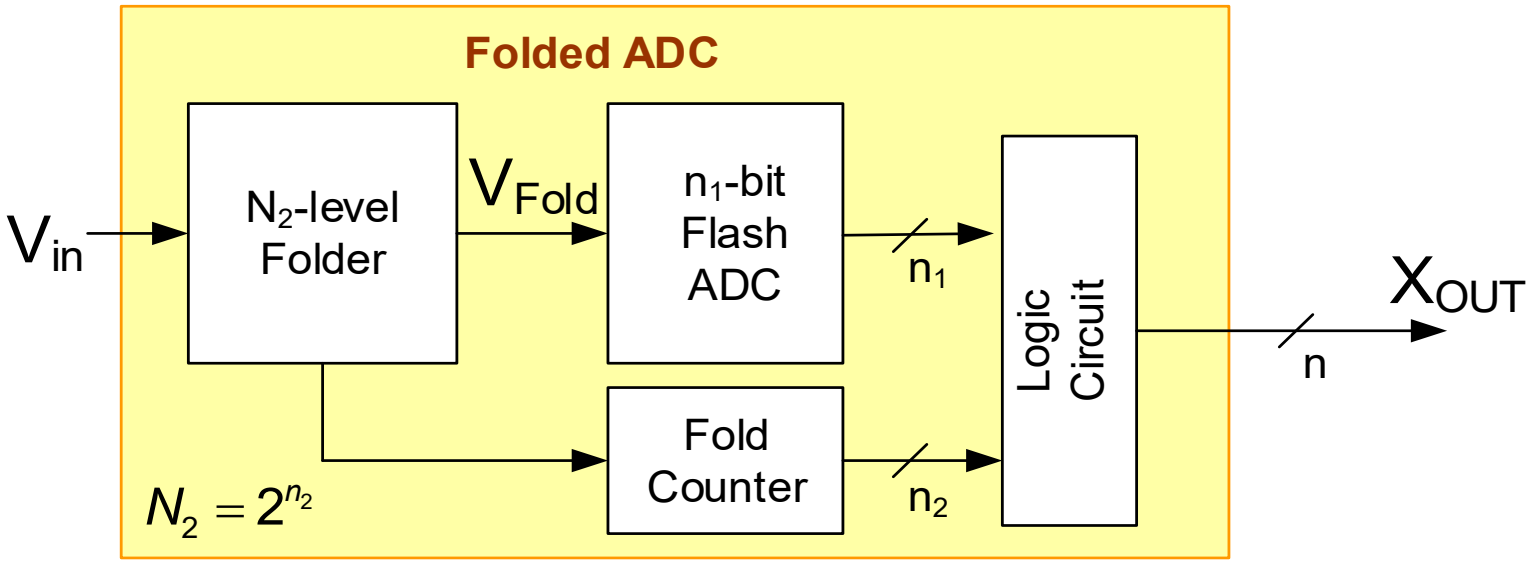
- Flash ADC has some really desirable properties (simple and fast)
- Wouldn't it be nice if we could derive most of the benefits of the FLASH ADC without the major limitations

To be practical at higher resolution, must address the major limitation of the FLASH ADC

Major Limitation of FLASH ADC at higher resolutions?

- **Number of comparators increases geometrically --- 2^n**
- **String DAC area increases geometrically**
- **Too many comparators making non-critical decisions increases power**

Folded ADC Architecture

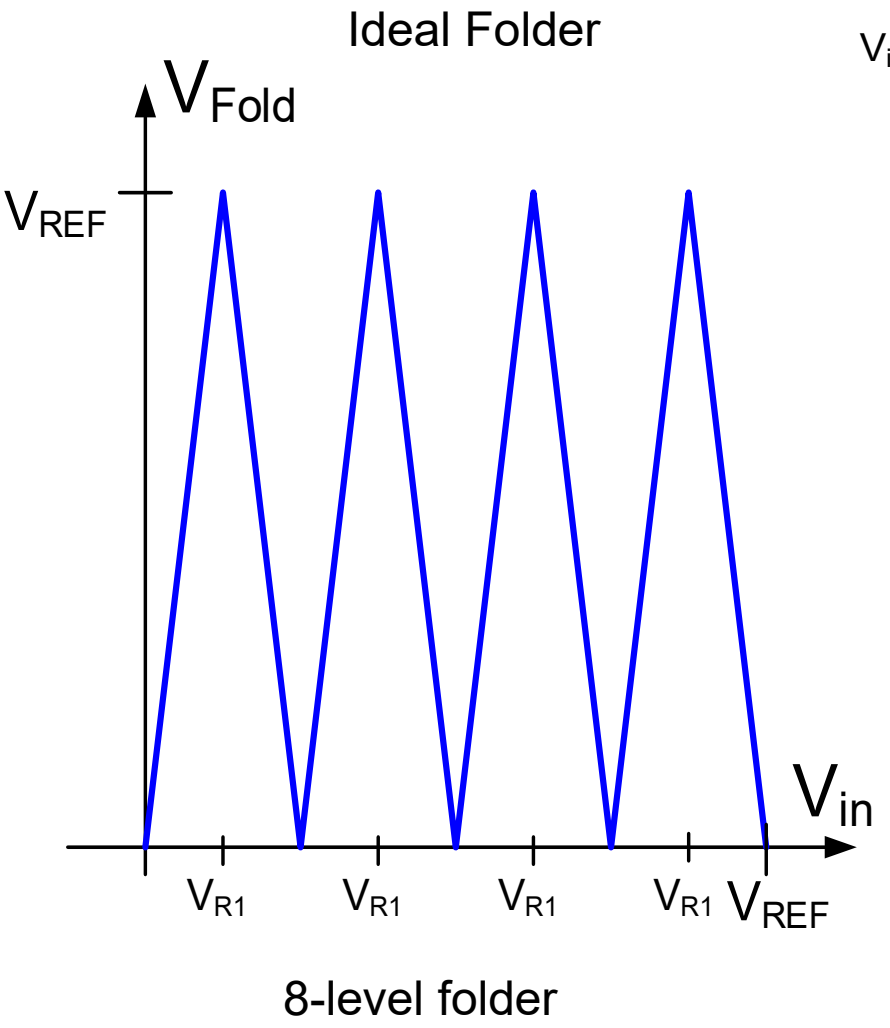


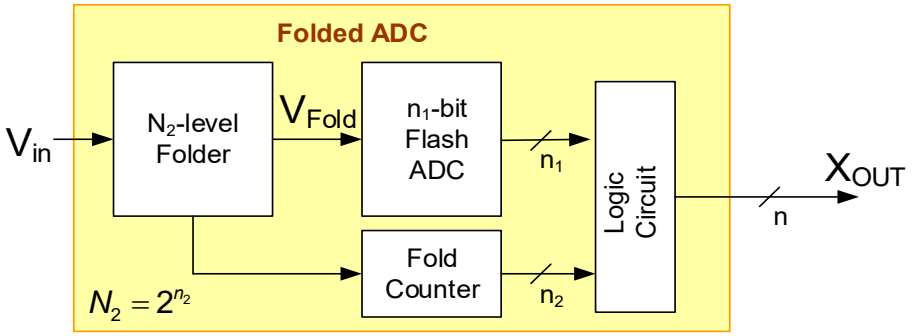
Premise: Folder provides large gain and is very fast

Similar in concept to interpolating flash ADC but

- Number of comparators has been reduced
- Thermometer to Binary decoder is eliminated

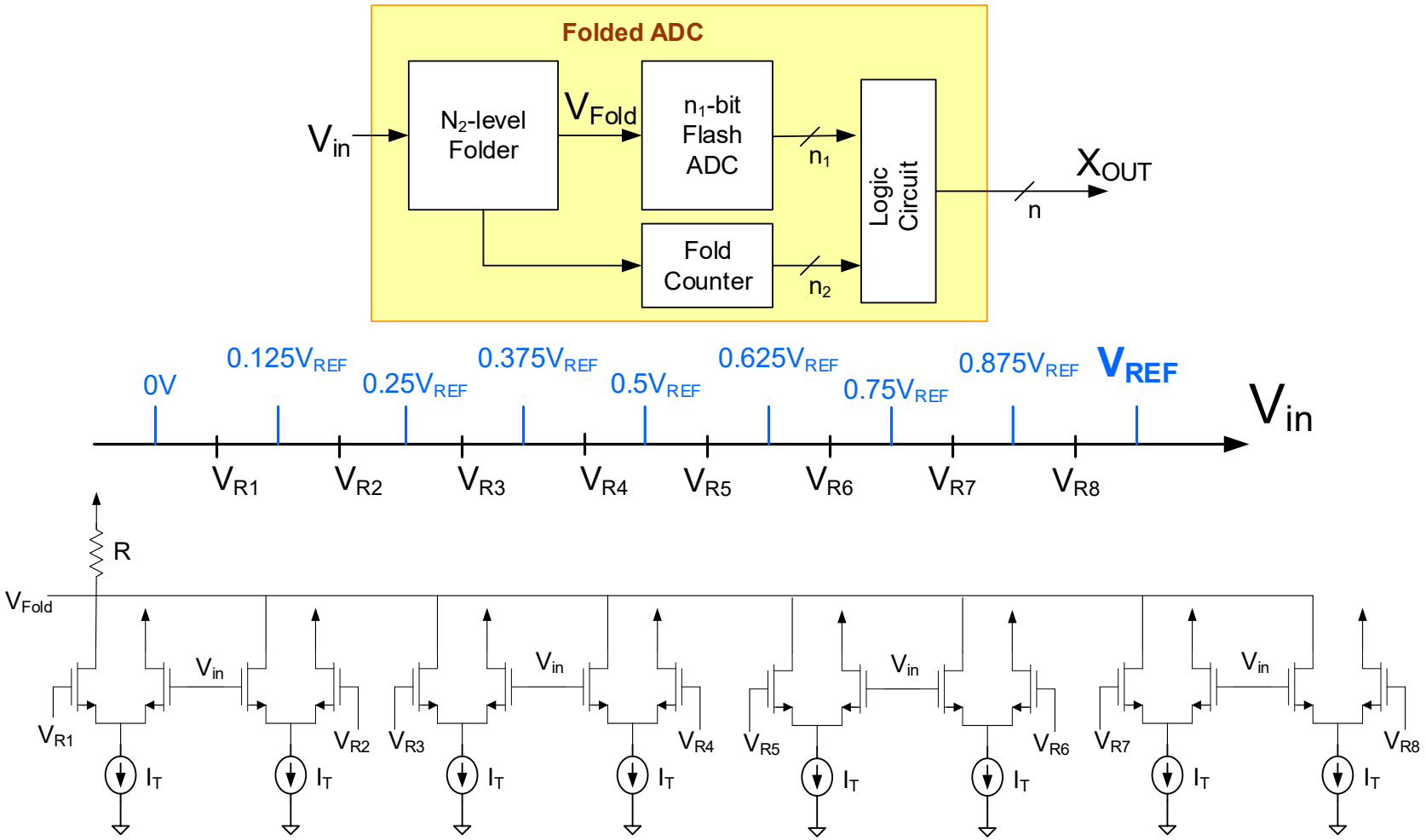
Folded ADC Architecture





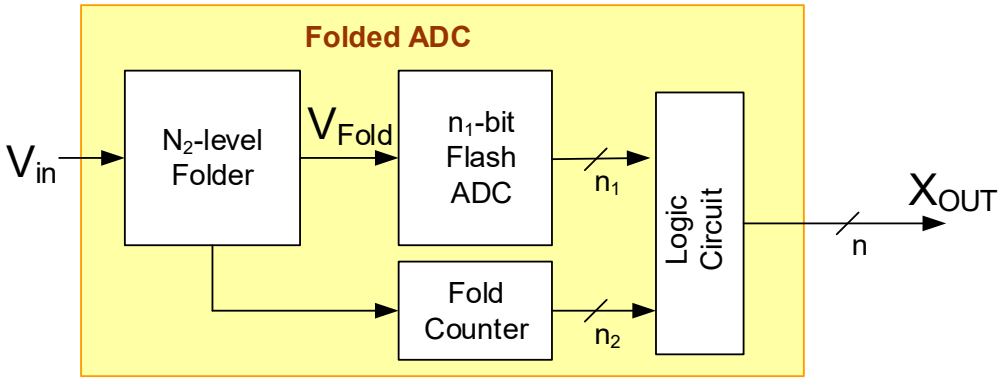
- Provides gain in each fold region
- Effective input range increased from V_{REF} to N_2V_{REF}
- Reduces performance requirements of flash ADC by N_2
- Reduces number of comparators by factor of N_2
- Performance strongly dependent upon performance of folder
- With fast folders, speed comparable to that of a flash ADC
- Architecture of choice by Phillips (now NXP) for high-speed operation for many years (Rudy van de Plassche)
- Competes with pipeline for performance

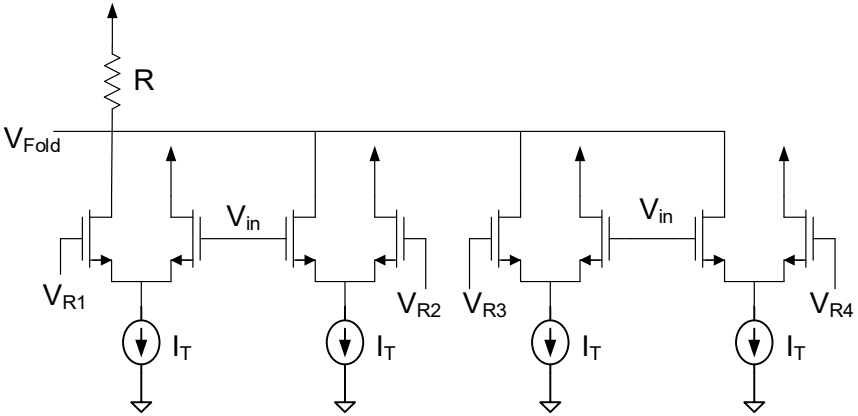
Folded ADC Architecture

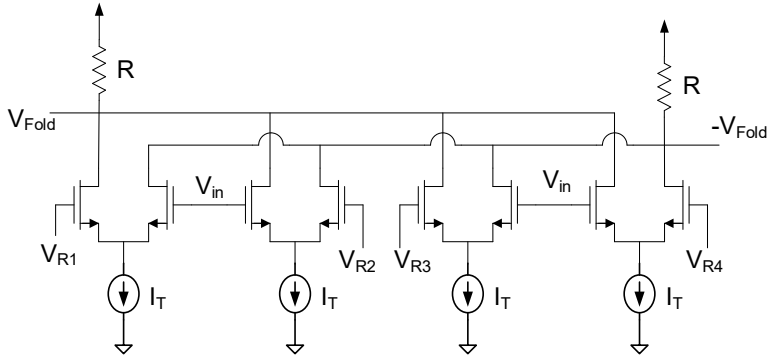


- Requires N_2 differential amplifiers
- Basic Folder Circuit (8 level)
- Simple Differential Pair can be very fast

Folded ADC Architecture



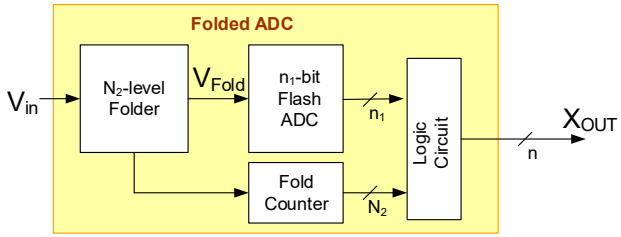




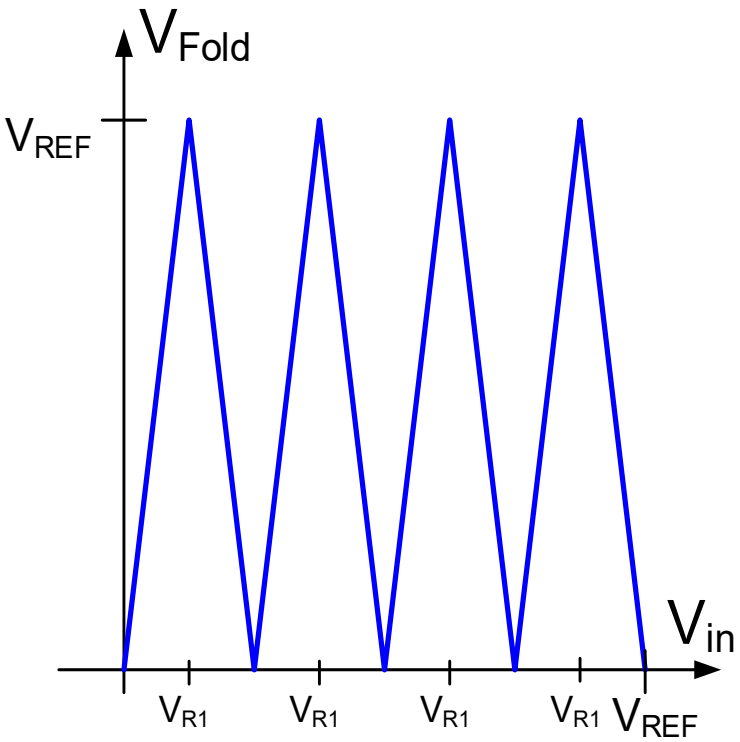
(Depicted for 4-level folder)

- Usually implemented in differential form
- Differential output almost free

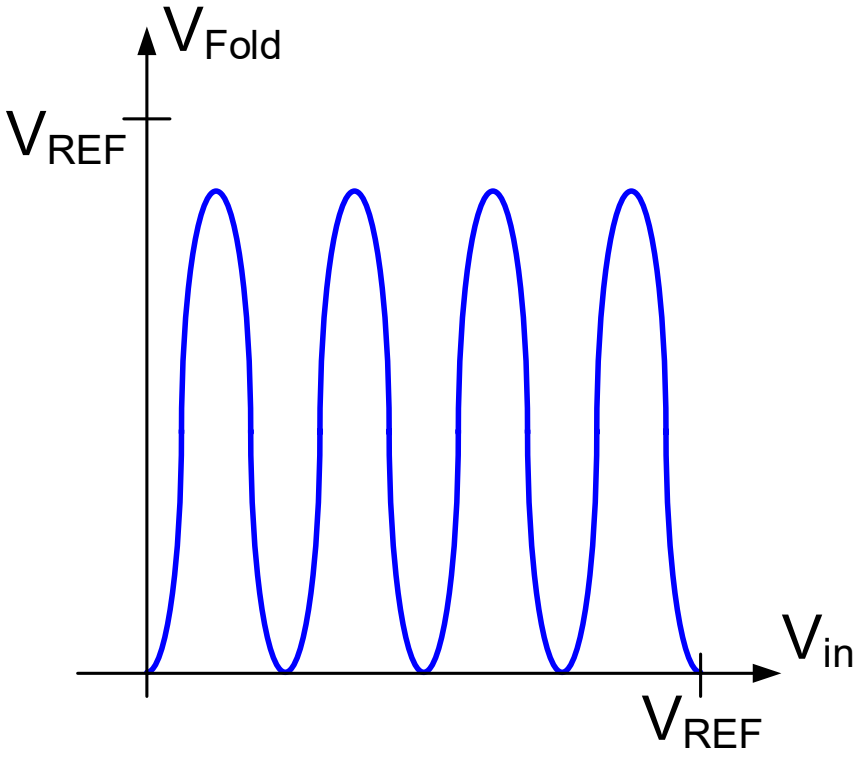
Folded ADC Architecture



Ideal Folder



Typical Folder



Nonlinearity in folder not a major problem since resolution nonlinearity affects primarily the LSBs and resolution of folded ADCs not large

Stay Safe and Stay Healthy !

End of Lecture 20